EMC-BASED MULTI-CORE CONTROL UNITS

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Abstract

Three various architectures are analysed targeting at implementing LUT-based circuits of control units. Each of them is based on a unique way of partial function generation. Depending on specifics of a control algorithm, one of these architectures provides minimum values of LUT counts. The methods target control blocks for electromagnetic compatibility of radiotechnical devices.

1. Introduction

One of the most basic problems connected with design of VLSI-based systems is providing the electromagnetic compatibility for different radiotechnical devices. This problem arises, for example, when the multi-block embedded systems are implemented [1]. Usage of various control units can help in solving this problem. The behaviour of control units (CU) can be defined by model of Mealy finite state machine (FSM) [2]. Nowadays, a lot of systems are implemented with FPGA chips. When their look-up table (LUT) elements are used, then a resulting circuit can have a lot of logic levels and spaghetti-type interconnections [3, 4]. To optimize the resulting FSM circuits, various methods of structural decomposition are used. Three possible architectures of LUT-based FSM circuits are analysed in this paper.

2. The background of a problem

Two systems of Boolean functions (SBFs) represent a logic circuit of Mealy FSM [5]. These SBFs represent input memory functions (IMFs) $\boldsymbol{D_r} \in \boldsymbol{D}$ and microoperations (MOs) $\boldsymbol{y_n} \in \boldsymbol{Y}$ [5]. Both SBFs depend on logic conditions (LCs) $\boldsymbol{x_l} \in \boldsymbol{X}$ and state variables $\boldsymbol{T_r} \in \boldsymbol{T}$. Let an FSM have $\boldsymbol{L}$ LCs, $\boldsymbol{N}$ MOs, $\boldsymbol{R}$ state variables and IMFs. To implement an FSM circuit, the SBFs are represented as sum-of-products having up to $\boldsymbol{L+R}$ literals. For complex FSMs, the values of $\boldsymbol{L+R}$ can reach 40-50.

The specific of LUT is a very small number of address inputs, $\boldsymbol{S_L}$ [5]. For a majority of practical FSMs, the following relation takes place:

$$\boldsymbol{L+R \gg S_L}. \quad (1)$$

If (1) holds, then the SBFs should be transformed using various methods of functional decomposition [2]. These methods produce multi-level LUT-based FSM circuits with rather sophisticated spaghetti-type interconnections [1]. In turn, this increases the power consumption and latency time of a CU.

The quality of an FSM circuit is determined by such values as [6]: the LUT count, maximum operating frequency, and power consumption. One of the ways leading to improving the FSM quality is changing its architecture. This can be done using methods of structural decomposition [2].

3. Main idea of proposed optimization methods

In this article, we propose to solve this problem using up to three types of state codes. They are used for generating partial Boolean functions (PBFs). These codes can be either maximum binary (MBC), or extended codes (ESC), or one-hot codes (OHC). Each of types determines a core of FSM circuit. As a result the set of FSM states $\boldsymbol{A = \{a_1, \dots, a_M\}}$ is divided by three sets. The belonging of the state $\boldsymbol{a_m}$ to a certain class is determined by $\boldsymbol{L_m}$. The value of $\boldsymbol{L_m}$ is equal to the number of LCs determining the transitions from the state $\boldsymbol{a_m}$.

If $\boldsymbol{L_m > S_L}$, then corresponding state belong to a class $\boldsymbol{A_{OH}}$. These states are encoded by OHCs. They

determine a core COH of a resulting FSM circuit. To implement the circuit of COH, it is necessary to use various methods of functional decomposition. This is the slowest part of an FSM circuit. It has the spaghetti-type interconnections.

If $L_m \leq S_L - R$, then corresponding state belong to a class A_{MB} . These states are encoded by MBCs. They determine a core CMB where there is no need in functional decomposition. To optimize the circuit of CMB, it is necessary to use various methods of optimal state assignment reducing the number of literals in corresponding SBFs. This is the fastest part of an FSM circuit. It has the regular-type interconnections.

If $L_m > S_L - R$, then corresponding state belong to a class A_{EC} . These states are encoded by partial codes which are combined into ESCs. They determine a core CEC. To implement this core circuit, there is no need in functional decomposition. But it is necessary to use an additional block transforming MBCs into ESCs [5, 6]. Due to it, the circuit of CEC is slower than the circuit of CMB. To optimize the circuit of CEC, it is necessary to use various methods of state distribution should be applied. These methods target at the circuit optimization for both CMB and CEC. This part of an FSM circuit has the regular-type interconnections.

In general case, the set A is represented as the union of three disjoint sets: $A = A_{OH} \cup A_{MB} \cup A_{EC}$. If all these sets are not empty, then an FSM circuit includes three cores with different partial Boolean functions. If only two of these sets are not empty, then the resulting circuit has two cores of logic. These cores determine the following vectors: $< A_{OH}, A_{MB} >$, $< A_{OH}, A_{EC} >$, $< A_{MD}, A_{EC} >$. In this case, the assembling of functions is necessary. If only a single set is not empty, then the corresponding FSM circuit has a single core. In this case, the assembling is necessary only in the case of ESCs. So, the final structure of FSM circuit depends on relations among the classes creating the set of states A.

4.Conclusion

Three different architectures of Mealy FSM logic circuits are discussed in this paper. They are based on using up to three different approaches of state assignment. As a result, an FSM circuit can include up to three cores. Each core generates partial Boolean functions depending on different state variables. If there is more than a single PBF core, then the final values of Boolean functions are implemented using a special assembling block. The proposed method presumes using the functional decomposition for a core based on one-hot state codes. To get the final values of extended state codes, the special code transformer should be used. It transforms MBCs into ESCs. This block consumes some resources of an FPGA chip. But the extended state codes are produced in parallel with output functions. This accelerates the FSM operation, but requires a lot of flip-flops. In turn, it leads to increasing the power consumption. Also, it increases the FSM operation cycle. If only MBCs are use, there is no need in the code transformation. In the best case, only MBCs are used. This is the best possible solution.

Our analysis helps to choose the best architecture of LUT-based FSM circuit. The multi-core approach can be used in the LUT-based optimization of various sequential devices providing electromagnetic compatibility in telecommunications.

References

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