CSC-BASED CONTROL ARCHITECTURES FOR EMC

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Abstract

Two new architectures are discussed which targets at implementing LUT-based circuits of control units. Each of them leads to different circuit of Mealy finite state machine. Depending on characteristics of an FSM, one of these approaches provides minimum LUT count. The methods target FSM providing control for electromagnetic compatibility of radiotechnical devices.

1. Introduction

One of the very important problems connected with FPGA-based design is the problem of providing the electromagnetic compatibility for different radiotechnical devices. This problem arises, for example, during the design of various embedded systems [1]. To solve this problem, various control blocks should be used. Very often, a model of Mealy finite state machine (FSM) [2] represents these sequential blocks. If circuits of these blocks are implemented using look-up table (LUT) elements, then a problem of LUT count reduction arises [3, 4]. This problem can be solved using various methods of state assignment. Some new methods are analysed in this paper.

2. Analysis of the problem

An FSM circuit is represented by two systems of Boolean functions (SBFs) [5]. These functions depend on external logical conditions $x_l \in X$ and internal state variables $T_r \in T$. These functions are input memory functions (IMFs) $D_r \in D$ and microoperations (MOs) $y_n \in Y$ [5]. As a rule, an FSM has L logical conditions, N MOs, R state variables and IMFs. These SBFs includes conjunctive terms which can include up to $L + R$ literals.

Modern LUTs have Th a very small number of inputs, S_L [5]. For real-life FSMs, the following relation holds:

$$L + R \gg S_L. \quad (1)$$

If (1) is true, then an FSM circuit is implemented using various methods of functional decomposition [2]. In this case, the resulting circuits are multi-level. It is known that such circuits are slow and have very high power consumption [1].

As a rule, quality of an FSM circuit depends on [2]: the LUT count, the maximum operating frequency, and the power consumption. To improve quality, LUT count and power should be minimized, whereas the frequency should be maximized. To do it, it is necessary to reduce the numbers of LUTs and their levels of FSM circuits.

3.Main idea of composite state assignment

In this article, we propose to solve this problem using methods of composite state assignment. In this case, it is necessary to create a partition $\Pi_A = \{A^1, \dots, A^K\}$ of the set of states $A = \{a_1, \dots, a_M\}$. This partition should include a minimum possible number of classes. The following condition should be satisfied for each class of Π_A:

$$R_S + L_k \le S_L. \quad (2)$$

In (2), R_S stands for the number of partial state variables used for encoding of the states $a_m \in A^k$, L_k stands for the number of FSM inputs determining transitions from the states $a_m \in A^k$.

In this case, an FSM circuit includes special blocks implementing the systems of partial functions

$$D^k = D^k(\tau_S, X^k); \quad (3)$$

$$Y^k = Y^k(\tau_S, X^k). \quad (4)$$

To implement systems (3)-(4), special blocks $LUTerk$ ($k \in \{1, \dots, K\}$) are introduced into an FSM circuit. Next, some block of function assembler implements the final values of $D_r \in D$ and $y_n \in Y$.

In this case, FSM states are represented by composite state codes (CSCs). Each CSC $CC(a_m)$ is a concatenation of class codes $K(A^k)$ and partial state odes $PC(a_m)$. These codes have $R_C + R_S = R_{CC}$ bits.

Two different approaches can be used for generating CSCs. Each of them results in the different architecture of an FSM structural diagram. Also, each approach produces FSM circuits with different values of LUT counts and operating frequencies.

In the first case, they are generated by a special block of code transformer. To implement this block, it is necessary to use additional LUTs and programmable interconnections. Obviously, this reduces the value of the maximum operating frequency. But this architecture is more flexible because maximum binary state codes can be used to implement multi-core control units. In multi-core architectures, a part of partial functions is based on maximum binary state codes.

In the second case, the CSCs are generated by the LUTs from the second logic level. Due to it, there is no code transformer. This approach allows maximum possible reducing the value of LUT count. Moreover, there are only two levels of logic in such circuits. But this architecture is rather rigid. It is impossible to implement various multi-core architectures using only composite state codes. So, this approach is suitable only for implementing single-core LUT-based FSM circuits.

4.Conclusion

Two different methods of FSM logic circuit organization are discussed in this paper. Each of them is based on using composite state codes for state assignment in LUT-based Mealy FSMs. The first architecture is based on transformation of maximum binary codes into CSCs. Having two types of state codes allows implementing multi-core circuits of LUT-based FSMs. But the code transformer consumes some additional LUTs and interconnections of an FPGA chip used. Also, it reduces the performance of resulting FSM circuit. In the second case, the composite state codes are produced together with microoperations. This accelerates the FSM operation. But this solution can be used only in the case of single-core FSM architectures.

Our research [2] shows that the final FSM circuit characteristics depend on the relation between the summarized numbers of state variables and logical conditions, on the one hand, and the number of LUT inputs, on the other hand. In some situations, the first architecture leads to FSM circuits with better LUT count. In other cases, the first architecture posses better characteristics. So, it is impossible to estimate the FSM circuit characteristics without implementing in using resources of a particular FPGA chip.

Our analysis helps to choose the best architecture based on composite state assignment This approach can be used in the LUT-based optimization of various sequential devices providing electromagnetic compatibility in telecommunications.

References

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