MC-BASED CONTROL UNITS FOR EMC

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Abstract

There is discussed a new architecture of FPGA-based control unit. The architecture targets at implementing LUT-based circuits of Mealy finite state machines (FSM).The proposed method is based on modification of composite state codes and encoding the collections of microoperations. The main goal of proposed approach is minimizing the nubmer of look-up (LUT) elements in FPGA-based circuit of control unit. The proposed approach targets FSM providing control for electromagnetic compatibility of radiotechnical devices.

1. Introduction

Using FPGA chips in logic design should take into account the problem of providing the electromagnetic compatibility for different radiotechnical devices. This problem arises, for example, during the design of various cyber-physical systems [1]. To solve this problem, sequential control blocks could be used. Very often, a model of Mealy finite state machine (FSM) [2] represents these sequential blocks. Mostly, the circuits of Mealy FSMs are implemented using look-up table (LUT) elements. In this case, the reducing problem of LUT count (the number of LUTs in a circuit) arises [3, 4]. This problem can be solved using various methods of state assignment. A new state assignment method is analysed in this paper.

2. Roots of the problem

A Mealy FSM circuit is represented by two systems of Boolean functions (SBFs) [5]. Each function depends on logical conditions $\boldsymbol{x_l} \in \boldsymbol{X}$ and state variables $\boldsymbol{T_r} \in \boldsymbol{T}$. The logical conditions show states of other system blocks. These functions are input memory functions (IMFs) $\boldsymbol{D_r} \in \boldsymbol{D}$ and microoperations (MOs) $\boldsymbol{y_n} \in \boldsymbol{Y}$ [5].The microoperations control other system blocks. Let an FSM have $\boldsymbol{L}$ logical conditions, $\boldsymbol{N}$ microoperations, $\boldsymbol{R}$ state variables and IMFs. In this case, both SBFs include conjunctive terms which consisting on up to $\boldsymbol{L} + \boldsymbol{R}$ literals.

Modern LUTs have a serious drawback: they have very small number of inputs, $\boldsymbol{S_L}$ [5]. Due to it, for complex FSMs, the following relation takes place:

$$\boldsymbol{L} + \boldsymbol{R} \gg \boldsymbol{S_L}. \tag{1}$$

If (1) is true, then an FSM circuit is implemented using various methods of functional decomposition [2]. In this case, the resulting circuits are multi-level. It is known that such circuits are slow and have very high power consumption [1]. To avoid this negative effect, the methods of structural decomposition should be applied [2].

The quality of FPGA-based FSM circuit mostly depends on three parameters [2]. They are the LUT count, the operating frequency, and the power consumption. To improve FSM circuit quality, it is necessary to minimize both LUT count and power consumption. At the same time, the FSM operating frequency should be maximized. This can be done using special methods of state assignment and encoding the collections of microoperations [2].

3.Main idea of proposed method

In this paper, we propose to solve this problem using modified method of composite state assignment. In this case, it is necessary to create a partition $\boldsymbol{\Pi_A} = \{\boldsymbol{A^1}, \dots, \boldsymbol{A^K}\}$ of the set of states $\boldsymbol{A} = \{\boldsymbol{a_1}, \dots, \boldsymbol{a_M}\}$. This partition should include a minimum possible number of classes. The following condition should be satisfied for each class of the partition Π_A:

$$R_S + L_k \le S_L. \tag{2}$$

In (2), the symbol R_S stands for the number of partial state variables used for encoding of the states $a_m \in A^k$, L_k stands for the number of FSM inputs determining transitions from the states $a_m \in A^k$.

We propose to use various numbers of bits for encoding the partial states for different classes of the partition Π_A. Next, we propose to encode the collections of microoperations. In this case, an FSM circuit includes K blocks implementing the systems of partial functions

$$D^k = D^k(\tau_S, X^k); \tag{3}$$

$$Y^k = Y^k(\tau_S, X^k). \tag{4}$$

Each system of partial functions (3)-(4) determines some blocks of LUTs denoted as $LUTerk$ ($k \in \{1, \dots, K\}$). These blocks create the first logic level of FSM circuit. Next, some block of function assembler implements the final values of input memory functions $D_r \in D$. The third logic level transforms the collections of MOs into the final values of microoperations $y_n \in Y$.

In this case, FSM states are represented by modified composite state codes (CSCs). The proposed codes have $R_C + R_S$= R_{CC} bits. The modified CSCs are generated by a special block of code transformer. To implement this block, it is necessary to use additional LUTs and programmable interconnections. Obviously, this reduces the value of the maximum operating frequency. Also, it is possible to generate the modified CSCs by the LUTs from the second logic level. This leads to excluding the circuit of code transformer. This approach allows maximum possible reducing the propagation time but it could increase the value of LUT count. The choice of the final method used is up to a control unit designer.

4. Conclusion

De facto, in this paper, we propose two different architectures of LUT-based FSM cirucit. Both architectures are based on modification of known composite state codes. Also, to minimize the LUT count, the method of encoding of collections of microoperations is applied. The first architecture is based on transformation of maximum binary codes into modified CSCs. This leads to using a code transformer. This is an overhead of this architecture. But this block does not increase the circuit delay, because the architecture includes a block of microoperations. In the second case, the modified composite state codes are produced together with codes of collections of microoperations. This solution eliminates the code transformer. But this solution cannot be used in the case of multi-core FSM architectures.

Our research [2] shows that the final FSM circuit characteristics depend on the relation between the summarized numbers of state variables and logical conditions, on the one hand, and the number of LUT inputs, on the other hand. In some situations, the first architecture leads to FSM circuits with a few elements. In other cases, the second architecture posses better spatial characteristics. Of course, the final characteristics of FSM cirucit depend on characteristics of the FPGA chip used.

Our analysis helps to choose the best architecture based on modified composite state assignment and encoding the collections of microoperations. This approach can be used in the FPGA-based optimization of various sequential blocks providing electromagnetic compatibility in telecommunications.

References

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